tion active devices. Metal lines **18** overlie a first interlevel dielectric **16** (e.g. of BPSG over TEOS), and make contact to active device areas at contact locations **20**. (This provides the starting structure on which planarization is performed as described above.) A planarization layer **22** is then deposited, by the techniques described above, to reduce or eliminate the topographical excursions of the structure. An interlevel dielectric **24** overlies the planarization layer **22** (and the rest of the planarized structure), and includes via holes **25** through which a second metal layer **26** contacts the first metal layer **18**. The structure shown can be topped by a protective overcoat (not shown) through which holes are etched to expose locations of contact pads in the second metal layer.

FURTHER MODIFICATIONS AND VARIATIONS

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

The disclosed innovative steps have been described in the context of via formation (e.g. forming connections from second metal to first metal, or third metal to second metal). Due to the accumulated topographical excursions, planarization is especially desirable at these stages. However, the disclosed innovative concepts can also be applied to planarization of lower levels as well.

The disclosed innovative concepts can also be applied to other spin-on materials, such as polyimide or polymethylmethacrylate.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

What is claimed is:

1. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer, to produce a stack including said third dielectric layer over said first and second dielectric layers;

(e.) performing a global etchback to substantially remove portions of said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining third dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

2. The integrated circuit of claim **1**, wherein said deposition step (c.) is plasma-enhanced.

3. The integrated circuit of claim **1**, wherein said deposition step (c.) uses TEOS as a source gas.

4. The integrated circuit of claim **1**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and Am before said deposition step (b.).

5. The integrated circuit of claim **1**, Hi wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

6. The integrated circuit of claim **1**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

7. The integrated circuit of claim **1**, wherein said interlevel dielectric is a doped silicate glass.

8. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing silicon dioxide, to form a second dielectric layer over said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second layers;

(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said spin-on glass of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining spin-on glass of said third dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

9. The integrated circuit of claim **8**, wherein said deposition step (c.) is plasma-enhanced.

10. The integrated circuit of claim **8**, wherein said deposition step (c.) uses TEOS as a source gas.

11. The integrated circuit of claim **8**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

12. The integrated circuit of claim **8**, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

13. The integrated circuit of claim **8**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

14. The integrated circuit of claim **8**, wherein said interlevel dielectric is a doped silicate glass.

15. An integrated circuit manufactured by the method comprising the acts of:

(a.) providing a partially fabricated integrated circuit structure;

(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material, to form a second dielectric layer over said first dielectric layer, said second dielectric layer having a thickness equal to or less than said first dielectric layer;

(d.) applying and curing spin-on glass, to form a third dielectric layer to produce a dielectric stack including said third dielectric layer over said first and second dielectric layers, said third dielectric layer having a thickness equal to or greater than said second layer;

(e.) performing a global etchback to substantially remove said dielectric stack from high points of said partially fabricated structure, wherein at least a portion of said third dielectric layer remains after said global etchback;

(f.) deposition of an interlevel dielectric at least over said remaining second dielectric layer;

(g.) etching holes in said interlevel dielectric in predetermined locations; and

(h.) depositing and patterning a metallization layer to form a desired pattern of connections, including connections through said holes.

16. The integrated circuit of claim **15**, wherein said deposition step (c.) is plasma-enhanced.

17. The integrated circuit of claim **15**, wherein said deposition step (c.) uses TEOS as a source gas.

18. The integrated circuit of claim **15**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. The integrated circuit of claim **15**, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

20. The integrated circuit of claim **15**, wherein said interlevel dielectric is a doped silicate glass.

21. The integrated circuit of claim **15**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

22. An integrated circuit, comprising:

(a.) an active device structure, including therein a substrate, active device structures, isolation structures, and one or more patterned thin film conductor layers including an uppermost conductor layer; and

(b.) a planarization structure, overlying recessed portions of said active device structure, comprising a layer of sol-gel-deposited dielectric overlain by a layer of vacuum-deposited dielectric overlain by a further layer of sol-gel-deposited dielectric;

(c.) an interlevel dielectric overlying said planarization structure and said active device structure, and having via holes therein which extend to selected locations of said uppermost conductor layer; and

(d.) an additional thin-film patterned conductor layer which overlies said interlevel dielectric and extends through said via holes to said selected locations of said uppermost conductor layer.

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